Question Bank (K Scheme)

Name of Subject: VLS   **Unit Test: II**

Subject Code: 316340   **Course : EJ6K**

Semester: VI

Unit - III Introduction to VLSI Design Concepts   16 Marks
2 Marks
1) Define:
a) Entity b) Architecture c) Configuration d) package e) library
2) What is the difference between VHDL and Verilog?
3) List any two arithmetic operators in VHDL.
4) List any two logical operators in VHDL.
4 Marks
1) State the use and syntax of a) Signal b) Variable c) Constant
2) Compare VHDL and Verilog
3) Explain entity and architecture with an example.
4) Explain VHDL data types with examples.
5) Differentiate between signal and variable.
6) Explain the different VHDL objects: signal, variable, and constant.
7) Explain enumerated data types and their applications.
8) Explain arithmetic operators in VHDL with examples.
9) Describe relational and logical operators in VHDL.
10) Explain shift operators used in VHDL.

Chapter 4: VHDL Programming   20 M

2 Marks
  1) State different modelling styles used in VHDL?
  2) State the difference between concurrent and sequential statements?
  3) Define data flow, behavioral and structural modeling.
  4) Define: a)Test bench b)Process

4 Marks
  1) Compare data flow, behavioral and structural modeling.
  2) Write the VHDL code to implement the 8:1multiplexer logic.
  3) Write a VHDL code for 3:8 decoder
  4) Write VHDL code for 8:3 encoder

5) Write 4:1 MUX code in VHDL Using case statement
6) Write VHDL code for D flip flop
7) Describe the following statement with example;
   (i) Assert statement (ii) wait statement (iii) case statement
8) Explain data flow modelling style with example
9) Explain structural modelling style with example
10) Explain concurrent constructs in VHDL.
11) Explain sequential constructs in VHDL.
12) Write a test bench code for full adder.
13) Write a test bench code for T flipflop.
14) Write VHDL code for 3 bit upcounter.

Chapter 5: HDL Simulation AND Synthesis   10M
2 Marks

1) Define event- based simulator and cycled-based simulator.
2) Define a)sensitivity list b) simulation cycle.
3) State components of simulation.
4) State HDL synthesis process.

4 Marks
1) Explain HDL design flow for synthesis.
2) Explain VLSI design flow.
3) Compare event- based simulator and cycled-based simulator.
4) Explain efficient coding styles rules.
5) Define synthesis? Explain synthesis issues in brief.
6) Explain the concept of delta delay.
7) Compare software and hardware description language